Intel HPC Technologies

Dr. Stephen Wheat
Intel, HPC Solutions

2014 Oklahoma Supercomputing Symposium

Norman, OK

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1 TRILLION

(10^{12})

1 TRILLION

(10^{12})

projected number of connected
machines and devices by 2022

Source: Trillion Sensors Summit, October 2013

40%

OF **FORTUNE500** COMPANIES IN **2000**
WERE OUT IN **2010**

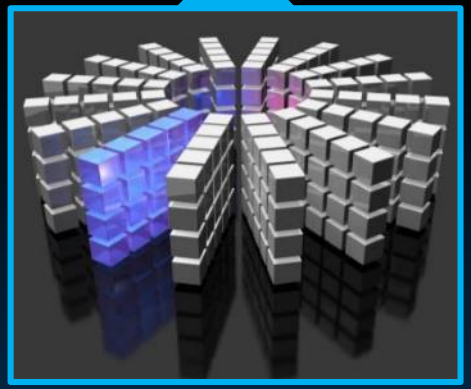
To Compete You Must Compute.

Intel in the Datacenter

CLOUD
Platform

BIG DATA
Platform

TC/HPC
Platform



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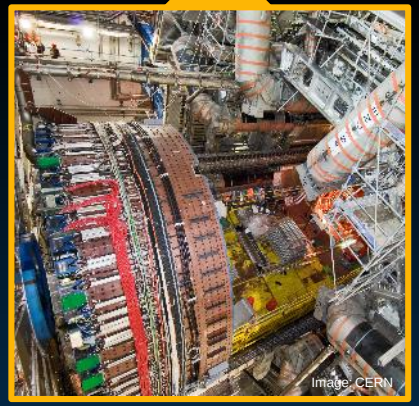
The Path to Discovery & Innovation

EXPERIMENT
Observation



THEORY
Mathematical Model

$$\left.\frac{\partial u_r}{\partial \theta}+\frac{u_\phi}{r}\frac{\partial u_r}{\partial \phi}-\frac{u_\theta^2+u_\phi^2}{r}\right)=-\frac{\partial p}{\partial r}+\rho g_r$$

$$\frac{1}{\sin(\phi)^2}\frac{\partial^2 u_r}{\partial \theta^2}+\frac{1}{r^2\sin(\phi)}\frac{\partial}{\partial \phi}\left(\sin(\phi)\frac{\partial u_r}{\partial \phi}\right)-2\frac{u_r+\frac{\partial u_\phi}{\partial \phi}+u_\phi}{r^2}$$

$$\left.\frac{\partial u_\theta}{\partial \theta}+\frac{u_\phi}{r}\frac{\partial u_\theta}{\partial \phi}+\frac{u_r u_\theta+u_\theta u_\phi\cot(\phi)}{r}\right)=-\frac{1}{r\sin(\phi)}\frac{\partial p}{\partial \theta}+\rho g_\theta$$

$$\frac{1}{\sin(\phi)^2}\frac{\partial^2 u_\theta}{\partial \theta^2}+\frac{1}{r^2\sin(\phi)}\frac{\partial}{\partial \phi}\left(\sin(\phi)\frac{\partial u_\theta}{\partial \phi}\right)+\frac{2\frac{\partial u_r}{\partial \theta}+2\cos(\phi)}{r^2\sin(\phi)}$$

$$\left.\frac{\partial u_\phi}{\partial \theta}+\frac{u_\phi}{r}\frac{\partial u_\phi}{\partial \phi}+\frac{u_r u_\phi-u_\theta^2\cot(\phi)}{r}\right)=-\frac{1}{r}\frac{\partial p}{\partial \phi}+\rho g_\phi$$

$$\frac{1}{\sin(\phi)^2}\frac{\partial^2 u_\phi}{\partial \theta^2}+\frac{1}{r^2\sin(\phi)}\frac{\partial}{\partial \phi}\left(\sin(\phi)\frac{\partial u_\phi}{\partial \phi}\right)+\frac{2}{r^2}\frac{\partial u_r}{\partial \phi}-\frac{u_\phi+}{r^2}$$

TC/HPC
Numerical Simulation

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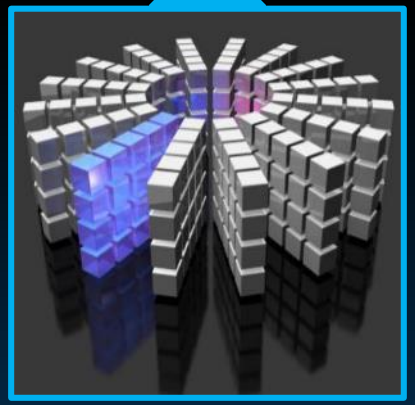
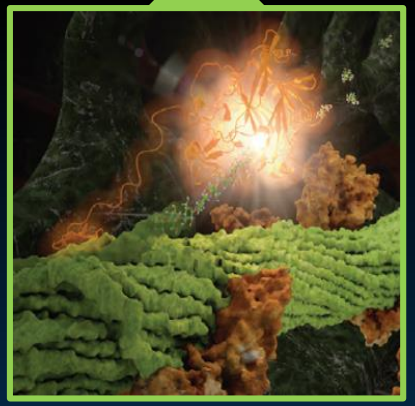
The Path to Discovery & Innovation

TECH COMPUTING / HPC

Numerical Simulation | Big Data Analytics | Visualization





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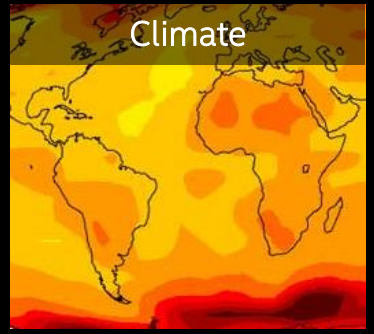
HPC Led Discoveries



www.hpcwire.com/2014/01/02/top-supercomputing-discoveries-2013/

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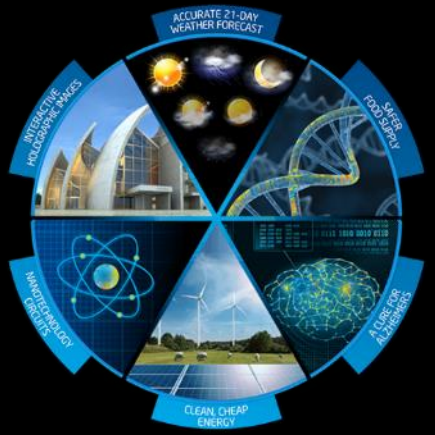
What does it mean?

for Science, Industry and Economics



- Better products – faster and cheaper
- Safer transportation (cars, trains, airplanes, boats, …)
- Better and more robust structures (bridges, buildings, machinery, …)
- Better materials and reduced material scrapping
- Resource efficient material
- Secure, clean, efficient ans sustainable energy
- Reducing fuel consumption and CO_2 emission (fuel efficiency)
- Generate more Oil&Gas reserves
- New energy resources (solar, wind, hydro)
- Improved Weather, severe storm, fire, flooding and earthquake prediction (catastrophe prevention)
- Better Disease control (fewer diseases and lower costs)
- Improved cancer treatment
- Better medicine, well-being, healthcare
- Better Bio-Economy (food&water security, sustainable agriculture)
- Better Cyber Security and electronic fraud control

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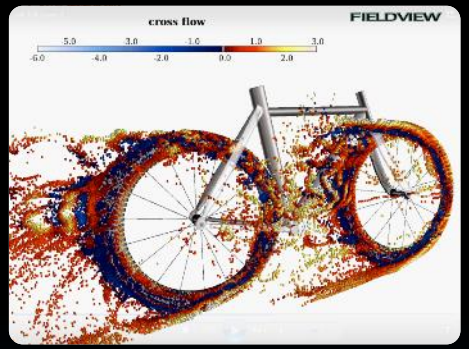
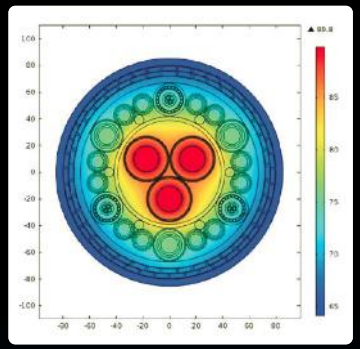
HPC Opportunites for SMBs





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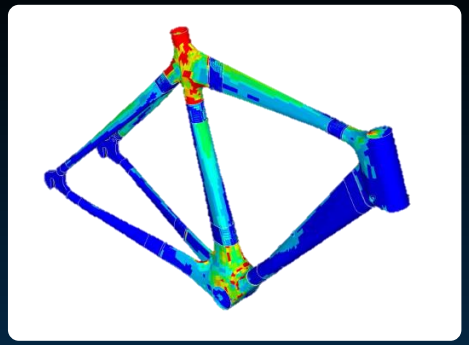

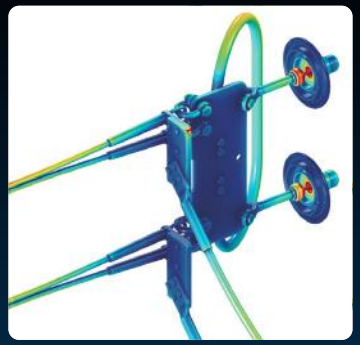

Better Products
More Producs

More Features

Faster Time to Market

More Efficient
Cheaper

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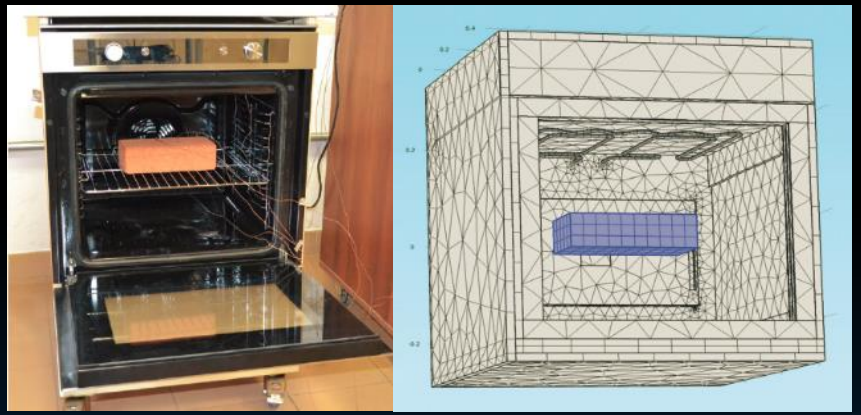
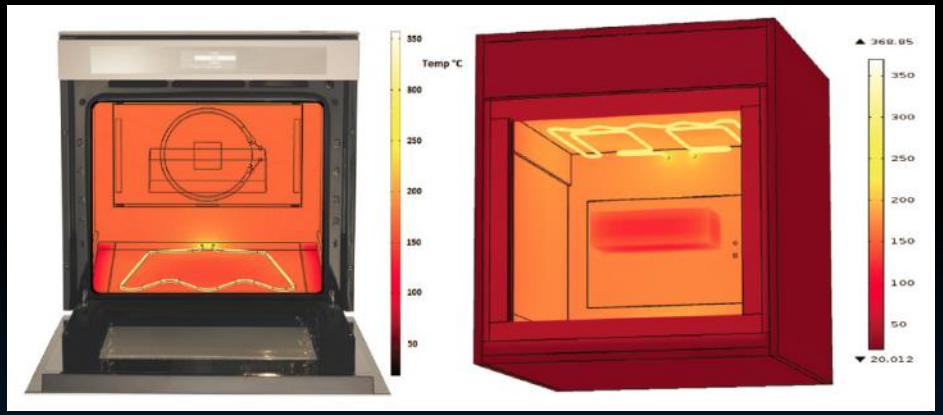
HPC Opportunities for SMB

Multiphysics Simulations





http://cdn.comsol.com/multiphysicssimulation/IEEE_Spectrum_Multiphysics_Simulation_2014.pdf

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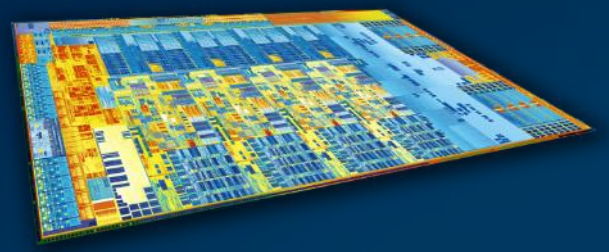
High Performance Computing (HPC)

- Addresses the world's hardest computational problems
- Performed on high-performance server nodes connected with high-performance fabrics

The Cluster is the System

STRATEGY:

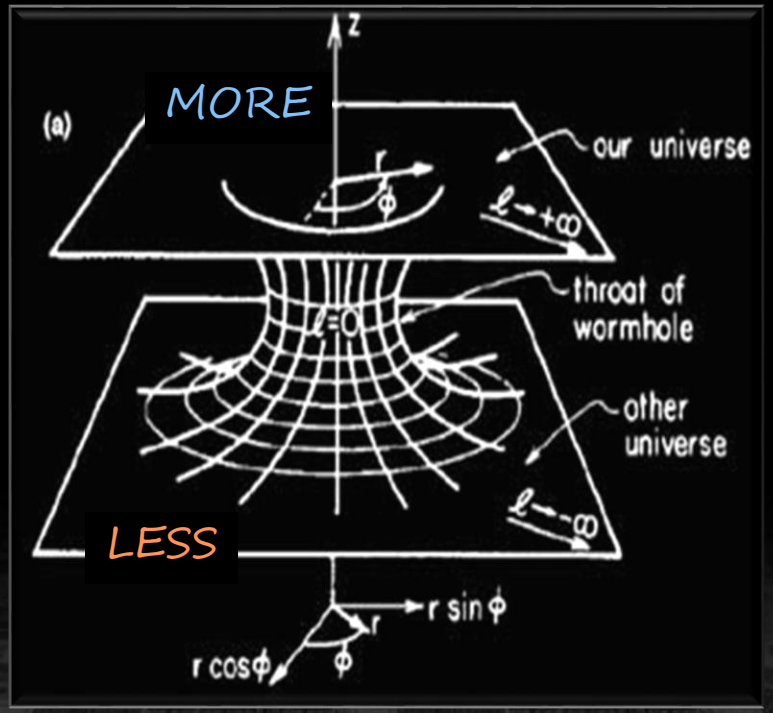
If it computes, it does it best with Intel




HPC IMPERATIVES
High Performance
Capabilities & Capacity
Energy Efficiency
TCO
Ease of Use
Productivity & Sustainability

Two Computing/Competing Universes

More Performance
More Memory
More Bandwidth
More Storage
More Speed
More Resiliency
More …



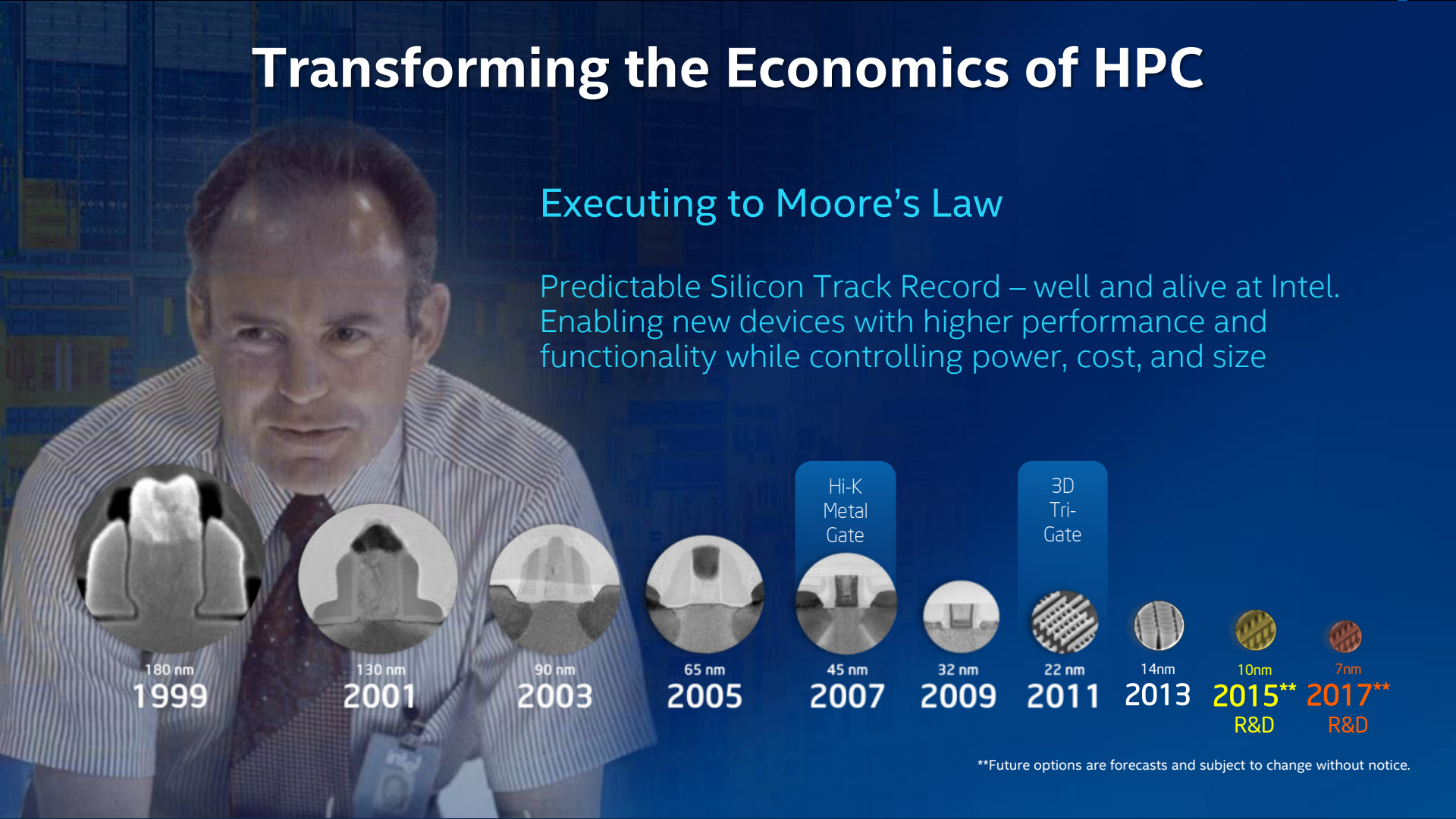
Less Power
Less Space
Less Complexity
Less Programming
Less Management
Less Costs
Less …

Integrated **El**ectronics

Transforming the Economics of HPC

Executing to Moore's Law

Predictable Silicon Track Record – well and alive at Intel.
Enabling new devices with higher performance and functionality while controlling power, cost, and size



**Future options are forecasts and subject to change without notice.

First Conflict-Free Processors

Photo: Sasha Lezhnev

World's First Conflict-Free Microprocessors[1]

What are Conflict Minerals?

Conflict Minerals are metals that come from the Democratic Republic of Congo (DRC), a place where violent militias and rebel groups control trade, exploit workers, and finance violence.

What has Intel done?

Intel, along with partners, created an audit and verification system that supports responsible sourcing of minerals from the DRC and the pursuit of conflict-free supply chains.

[1] Intel has manufactured the world's first commercially available "conflict-free" processors. "Conflict-free" means "DRC conflict-free", which is defined by the Securities and Exchange Commission rules to mean products that do not contain conflict minerals (tin, tantalum, tungsten and/or gold) that directly or indirectly finance or benefit armed groups in the Democratic Republic of the Congo (DRC) or adjoining countries.

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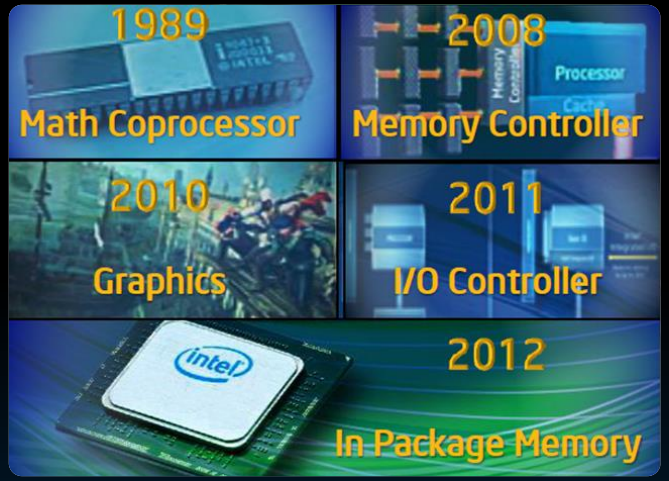
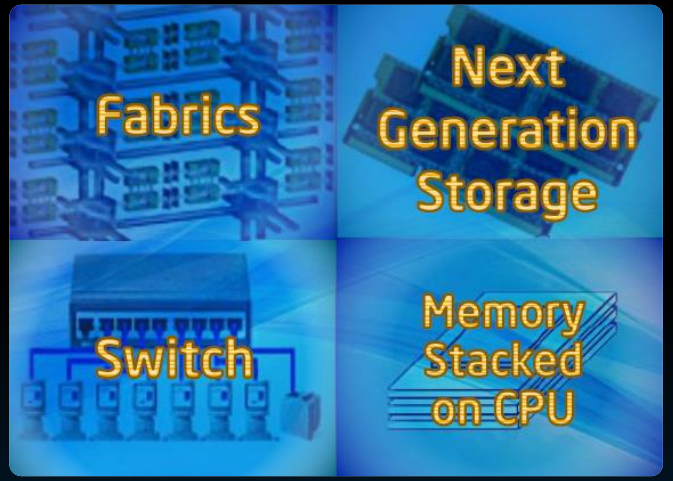
Driving Innovation and Integration

Enabled by Leading Edge Process Technologies



Integrated Today



Coming Tomorrow**

SYSTEM LEVEL BENEFITS IN COST, POWER, DENSITY, SCALABILITY & PERFORMANCE

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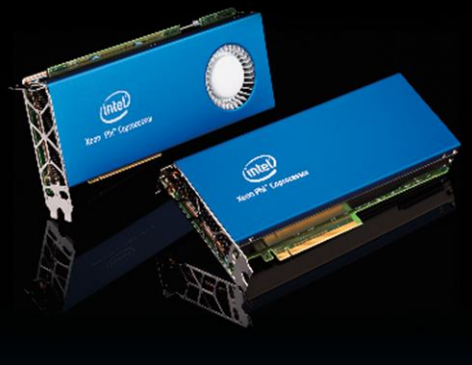
From MILLIWATTS to TERAFLOPS

Smartphones
with Intel® Inside

Intel® Xeon®
Processors



Intel® Many Integrated Core
Architecture

Energy Efficient

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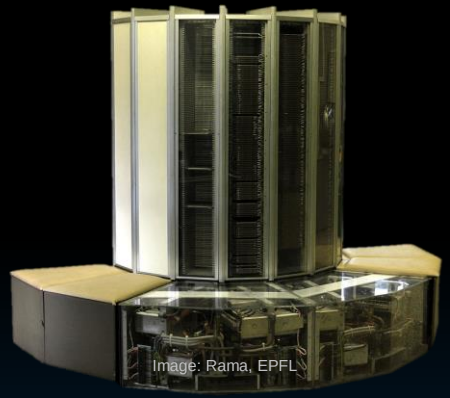
The Magic of Integration

Moore's Law at Work & Architecture Innovations



6666x

1970s

150 MFLOPS

CRAY-1*

2013

1000000 MFLOPS

Intel® Xeon Phi™

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Intel Technical Computing

The Right Tool for the Job: A Continuum of Computing

Desktop

Tablet

See a simple result

Intel® Xeon® Workstation

More results, faster
Better teamwork
Faster turns

Local Cluster Computation

More simulations
Breakthrough ideas
& research

Large Clusters

Change the world
Discover the unknown
Transformational insight

Common underlying architecture
scales investments across technical computing platforms

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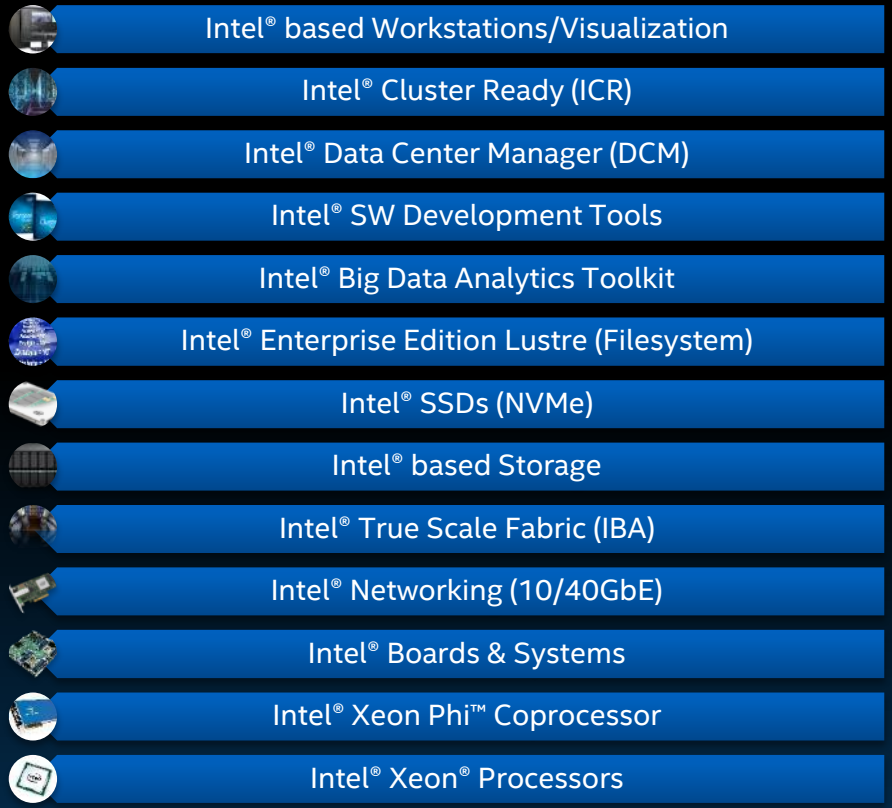
Intel Technical Computing Portfolio



INTEL TECHNICAL COMPUTING & HPC SOLUTIONS PORTFOLIO

All components working "better together" for a comprehensive and high-performance end-to-end solution based on Intel technologies

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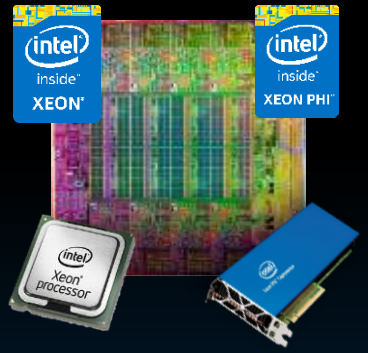
Intel Technical Computing & HPC

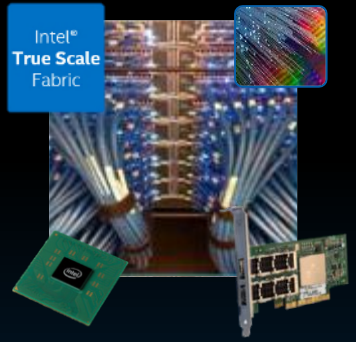
Technologies

Compute Processing



Systems & Boards

Network & Fabric



I/O & Storage

Software & Services

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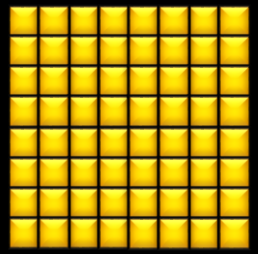
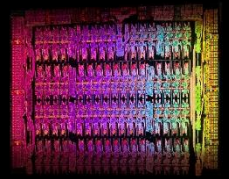
„Big Core“ – „Small Core“

Different Optimization Points
Common Programming Models
and Architectural Elements





Intel® Xeon® Processor

Simply aggregating more cores generation after generation is not sufficient

Performance per core/thread must increase each generation, be as fast as possible

Power envelopes should stay flat or go down each generation

Balanced platform (Memory, I/O, Compute)

Cores, Threads, Caches, SIMD

Intel® Xeon Phi™ Coprocessor

Optimized for highest compute per watt

Willing to trade performance per core/thread for aggregate performance

Power envelopes should also stay flat or go down every generation

Optimized for highly parallel workloads

Cores, Threads, Caches, SIMD

For illustration only

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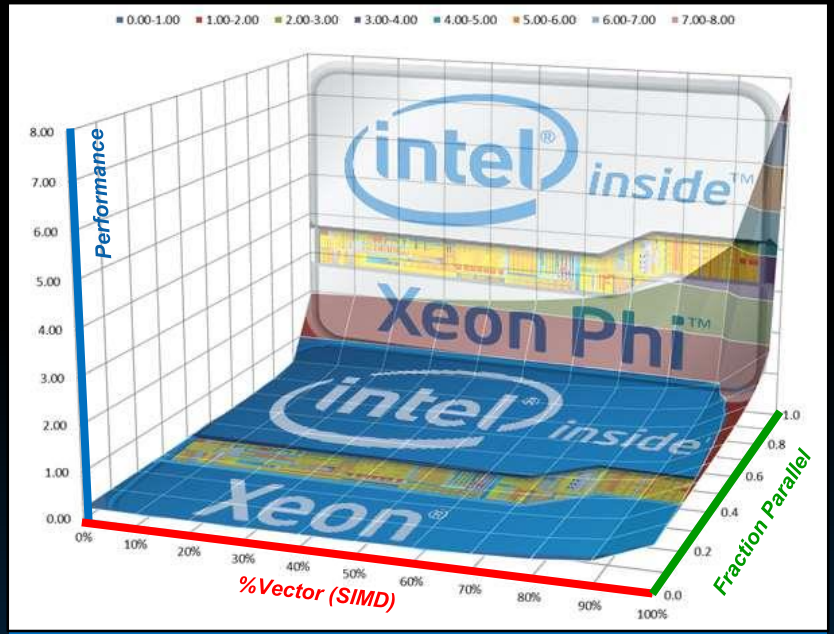
Modernize Your Software !

Performance = Parallelism on all Levels



Theoretical acceleration of a highly parallel processor over a Intel® Xeon® parallel processor (<1: Intel® Xeon® faster) – For illustration only

NODES clustering

SIMD vectorization

CORES multi-threading

ILP instruction parallelism

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Parallel is Your Path Forward

General Purpose and Fully Programmable Hardware

Industry Standards Software and Tools

Productive and Sustainable

Did you know?

All modern processors and systems use parallelism for performance.

Common Programming Models & Software Tools

Common Intel® architecture enables applications to run across the full spectrum of Intel® Xeon® family based servers so programmers don't have to "start over".

Cluster Edition
Professional Edition

Use the same development tools you used for Intel® Xeon® processors with Intel® Parallel Studio XE 2015

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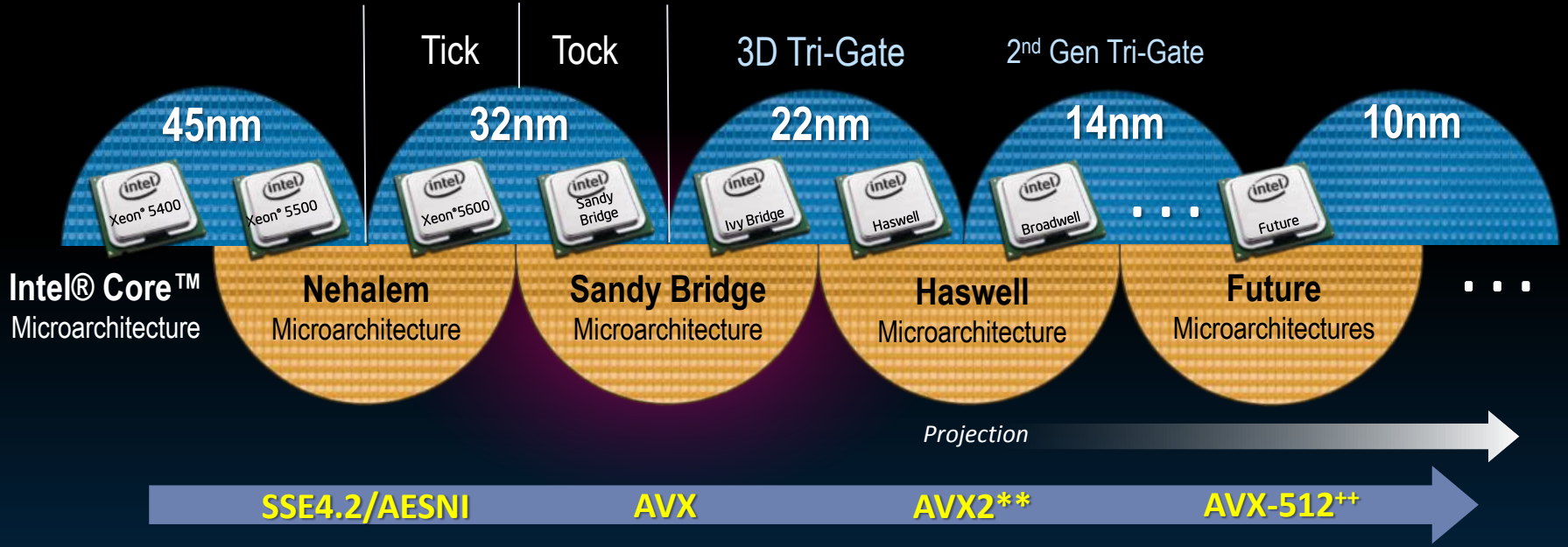
Tick-Tock Development Cycles

Integrate. Innovate.



**Intel® Architecture Instruction Set Extensions Programming Reference, #319433-012A, FEBRUARY 2012

++Intel® Architecture Instruction Set Extensions Programming Reference, #319433-015, JULY 2013

Potential future options, subject to change without notice.

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Intel® Xeon® Processor E5-2600 v2

„Ivy Bridge EP“

3D Tri-Gate
22nm
Process

ISA
AVX
SIMD-256

Up to
12 Cores
24 Threads

Up to
3.5 GHz
Base Frequency

Up to
30 MB
L3-Cache

Up to
1866 MHz
DDR3 Memory

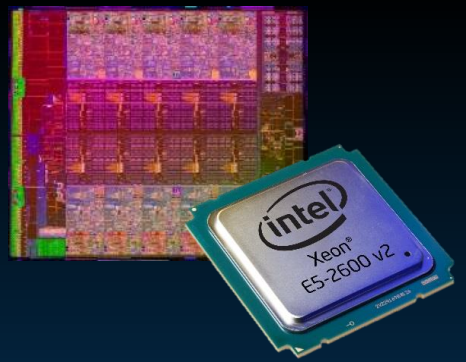
Up to
768 GB
Memory Capacity†

Up to
8.0 GT/s
QPI

Integrated
40 Lanes
PCIe* 3

Standard Processor
60-130 W
TDP

Up to
259 GFLOPS
(DP-F.P. peak)



† depending DIMM capacity availability

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Intel® Xeon® Processor E5-2600 v3

„Haswell EP“

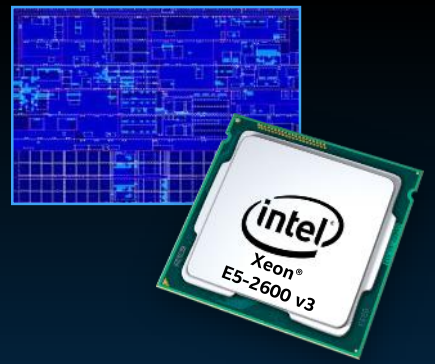
NEW

3D Tri-Gate **22 nm** Process	ISA **AVX2** SIMD-256	New **TSX** Transactional Synch
Up to **18 Cores** 36 Threads	Up to **3.5 GHz** Base Frequency	Up to **45 MB** Shared L3-Cache
Up to **2133 MHz** DDR4 Memory	Up to **768 GB** Memory Capacity	Up to **68.2 GB/s** Peak Memory Bandwidth
Integrated **40 PCIe*3** Lanes (40GB/s)	Up to **9.6 GT/s** QPI (2x)	Standard Processor **60-145 W** TDP (with integrated VR)

Up to

500+ GFLOPS

(DP-F.P. peak)



Potential future options, subject to change without notice. Codenames.
All timeframes, features, products and dates are preliminary forecasts and subject to change without further notification.

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Announcing

Intel® Omni Scale—The Next-Generation Fabric

- Designed for Maximum Scalability
- Rich Set of Programming Models
- Flexible Configurations
- End-to-End Solution

INTEGRATION

Intel® Omni Scale Fabric

Starting with Knights Landing

Intel® Omni Scale Fabric

Future 14nm generation

Coming in '15

√ PCIe Adapters √ Edge Switches √ Director Systems √ Intel Silicon Photonics √ Open Software Tools*

Intel® True Scale Fabric Upgrade Program *Helps Your Transition*

*OpenFabrics Alliance

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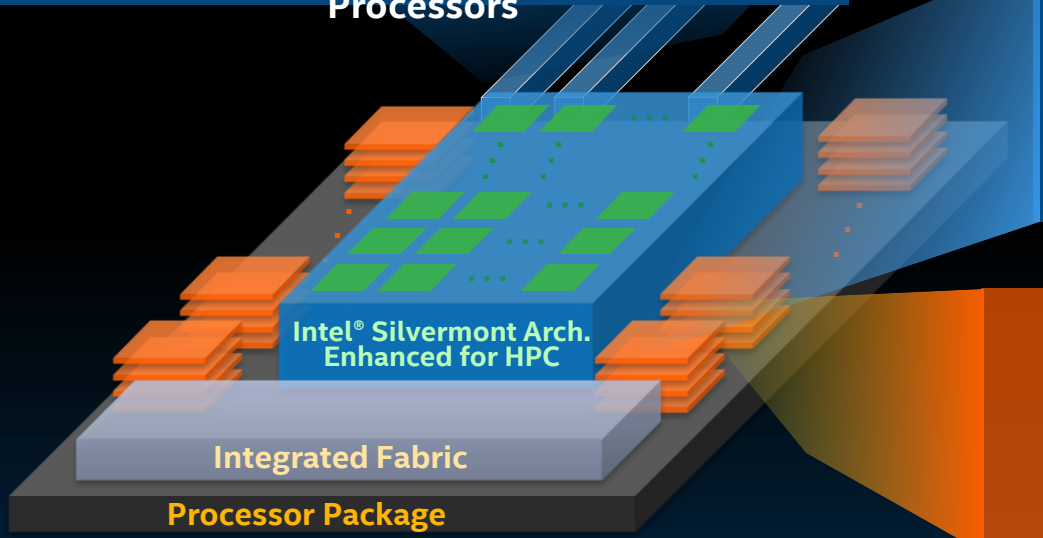
Unveiling Details of Knights Landing

(Next Generation Intel® Xeon Phi™ Products)

2nd half '15
1st commercial systems

3+ TFLOPS[1]
In One Package
Parallel Performance & Density

Platform Memory: DDR4 Bandwidth and Capacity Comparable to Intel® Xeon® Processors



Compute: Energy-efficient IA cores[2]

- *Microarchitecture enhanced for HPC[3]*
- *3X Single Thread Performance vs Knights Corner[4]*
- *Intel Xeon Processor Binary Compatible[5]*

On-Package Memory:

- *up to 16GB at launch*
- *1/3X the Space[6]*
- *5X Bandwidth vs DDR4[7]*
- *5X Power Efficiency[6]*

Jointly Developed with Micron Technology

All products, computer systems, dates and figures specified are preliminary based on current expectations, and are subject to change without notice. [1]Over 3 Teraflops of peak theoretical double-precision performance is preliminary and based on current expectations of cores, clock frequency and floating point operations per cycle. FLOPS = cores x clock frequency x floating-point operations per second per cycle. . [2]Modified version of Intel® Silvermont microarchitecture currently found in Intel® Atom™ processors. [3]Modifications include AVX512 and 4 threads/core support. [4]Projected peak theoretical single-thread performance relative to 1st Generation Intel® Xeon Phi™ Coprocessor 7120P (formerly codenamed Knights Corner). [5] Binary Compatible with Intel Xeon processors using Haswell Instruction Set (except TSX) . [6]Projected results based on internal Intel analysis of Knights Landing memory vs Knights Corner (GDDR5). [7]Projected result based on internal Intel analysis of STREAM benchmark using a Knights Landing processor with 16GB of ultra high-bandwidth versus DDR4 memory only with all channels populated.

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Conceptual—Not Actual Package Layout

Knights Landing

NERSC

40 YEARS at the FOREFRONT 1974-2014

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NERSC, CRAY, INTEL TO COLLABORATE ON NEXT-GENERATION SUPERCOMPUTER

APRIL 29, 2014 | Tags: NERSC
Contact: Jon Bashor, jbashor@lbl.gov, 510-486-5849

The U.S. Department of Energy's (DOE) National Energy Research Scientific Computing (NERSC) Center and Cray Inc. announced today that they have signed a contract for a next generation of supercomputer to enable scientific discovery at the DOE's Office of Science (DOE SC).

Lawrence Berkeley National Laboratory (Berkeley Lab), which manages NERSC, collaborated with Los Alamos National Laboratory and Sandia National Laboratories to develop the technical requirements for the system.

The new, next-generation Cray XC supercomputer will use Intel's next-generation Intel® Xeon Phi™ processor — code-named "Knights Landing" – a self-hosted, manycore processor with on-package high bandwidth memory and delivers more than 3 teraFLOPS of double-precision peak performance per single socket node. Scheduled for delivery in mid-2016, the new system will deliver 10x the sustained computing capability of NERSC's Hopper system, a Cray XE6 supercomputer.

NERSC serves as the DOE SC's primary high performance computing (HPC) facility, supporting more than 5,000 scientists annually on over 700 projects. The $70 million plus contract represents the DOE SC's ongoing commitment to enabling extreme-scale science to address challenges such as developing new energy sources, improving energy efficiency, understanding climate change, developing new materials

NERSC's next-generation supercomputer, a Cray XC, will be named after Gerty Cori, the first American woman to be honored with a Nobel Prize in science. She shared the

http://nnsa.energy.gov/mediaroom/pressreleases/04.01.10

Cray Wins $174 Million Contract For Trinity Supercomputer Based on Knights Landing

July 10, 2014 by Rich Brueckner | Leave a Comment

Today Cray announced the Company has been awarded one of the largest contracts in Cray's history — a $174 million deal to provide the NNSA with a next generation Cray XC supercomputer. As part of the Trinity procurement, the 15 Megawatt supercomputer will be based on Intel Knights Landing.

The next-generation Cray XC supercomputer will provide the NNSA with a world-class supercomputing system to advance the mission for the agency's stockpile stewardship program. The system, named "Trinity" by the NNSA, is a joint effort between the New Mexico Alliance for Computing at Extreme Scale (ACES) at the Los Alamos National Laboratory and Sandia National Laboratories as part of the NNSA Advanced Simulation and Computing Program (ASC). The new Cray supercomputer will be used to ensure the safety, security and effectiveness of the United States' nuclear stockpile.

http://insidehpc.com/2014/07/10/cray-wins-174-million-contract-trinity-supercomputer-based-knights-landing/

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AMBER WRF VISIT VASP UTBENCH SU2 SG++ SeisSol, GADGET, SG++ ROTOR SIM R Quantum Espresso Optimized integral OPENMP/ MPI Openflow NWChem

AVBP (Large Eddy) NEMO5

Modernizing Community Codes…*Together*

MPAS

Blast Mardyn

BUDE MACPO

CAM-5 Ls1

CASTEP Harmonie

Castep GTC

CESM GS2

CFSv2 Gromacs

CIRCAC GPAW

Intel® Parallel Computing Centers

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The University of Edinburgh
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ICHEC Irish Centre for High-End Computing
University of Bristol
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CSC
CISS
Institute of Industrial Science The University of Tokyo
UT
भारतीय विज्ञान संस्थान
Purdue University
The University of Wisconsin Madison
TACC
Stanford University
Berkeley Lab
Penn State
Georgia Tech
University of Colorado Boulder
NCAR
東京大学 The University of Tokyo
LSU Center for Computation & Technology Interdisciplinary | Innovative | Inventive

***Plus…*User Groups Forming**

CliPhi (COSMOS) COSA Cosmos codes DL-MESO DL-Poly ECHAM6 Elmer FrontFlow/Blue Code GADGET GAMESS-US

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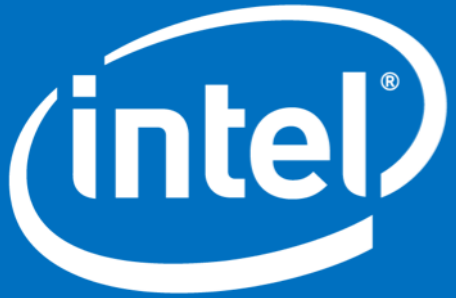
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